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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/600,875 | 06/20/2003 | Blaine Stackhouse | 200207083-1 | 6673 |

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

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| EXAMINER |
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NGUYEN, DANG T

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| ART UNIT | PAPER NUMBER |
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2824

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-----------------|-------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/600,875 | STACKHOUSE ET AL. | |
| | Examiner | Art Unit | |
| | Dang T. Nguyen | 2824 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-20 is/are allowed.
- 6) ☒ Claim(s) 1-8, 11 and 21-25 is/are rejected.
- 7) ☒ Claim(s) 9 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>Search history</u> . |

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 12/21/05.

Claims 1 – 25 are pending on this application. Claims 1, 6, 12, 17 and 21 are independent claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-8, 11 and 21-25 remain rejected under 35 U.S.C. 102(b) as being anticipated by Patel et al. U.S. patent No. 6,025,737 – filed: May 27, 1997.

Regarding independent claim 1, Fig. 10C of Patel et al. discloses a bias generator [1050, 1055] for testing (intended of use) of a static random access memory SRAM (Col. 7 lines 55 - 60) comprising: an output (To core) of the bias generator [1050,1055] and means [1060, 1064] (Col. 15 lines 50-52 and 62-64) for adjusting a set of available magnitudes at the output of a bias voltage output signal (To core) at the output using metal programming (Col. 15 lines 48 - 53).

Regarding dependent claim 3, Fig. 10C further discloses wherein the means for adjusting [1060, 1064] comprises a metal transistor (Col. 15 lines 48 - 53) in the bias generator [1050, 1055], the metal programmable transistor [1060,1064] comprising either or both of a metal-programmable pull-up transistor [1060] and a metal-

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programmable pull-down transistor [1064] that change one or both of a range and a resolution of the set of available magnitudes (To core) when the metal-programmable transistors [1060, 1064] is metal programmed (Fig.10D, 10E).

Regarding dependent claim 4, Fig. 10C et al. further comprising: a pull-up array of transistors [1062 ...] connected between a first supply voltage [VCCQ] and the bias generator output (To Core); a pull-down transistor [1066] connected between the bias generator output (To Core) and a second supply voltage [GROUND]; and a gate bias circuit (Fug, 10E [shift trip point down]) connected between a mode select input (Fig. 10E [Pin]) and a gate of the pull-down transistor [1064], wherein the metal-programmable pull-up transistor [1060] is connectable in parallel or in series with the pull-up transistor array [1062 ...], and wherein the metal-programmable pull-down transistor [1064] is connectable in parallel or in series with the pull-down transistor [1064].

Regarding dependent claim 5, Fig. 10C et al. further discloses wherein each of the metal-programmable pull-up transistor and the metal-programmable pull-down transistor [1060, 1064] has a respective ON state resistance that, when either or both are metal programmed, combines with an effective ON state resistance of the pull-up transistor array and an ON state resistance of the pull-down transistor [Fig. 10D, 10E] to adjust the set of available magnitudes.

Regarding dependent claim 6, Fig. 10C of Patel et al. discloses a bias generator [1050, 1055] for testing (intended of use) of a static random access memory SRAM (*Col. 7 lines 55 - 60*) comprising: a metal programmable transistor [1060, 1064] that adjusts a set of available magnitudes of a bias voltage output signal (To Core) at

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the bias generator output (output of 1050, 1055) when metal programmed (Fig. 10D, 10E).

Regarding dependent claims 7 and 8, the claims incorporated the same subject matter as of claims 3 and 4, and rejected along the same rationale.

Regarding dependent claim 11, Fig. 10C further discloses wherein the pull-up array transistors are p- type metal oxide semiconductor transistors [1062....] that function to pull up [VCCQ] the bias voltage output signal [To Core] when in an ON state (Fig. 10), and wherein the pull-down transistor is an n-type metal oxide semiconductor transistors [1062] that functions to pull down the bias voltage output signal to the second supply voltage [Ground] when in the ON state (Fig. 10E), the second supply voltage [Ground] being less than the first supply voltage [VCCQ], the second supply voltage optionally being zero volts or a ground voltage [Ground].

Regarding dependent claim 21, Fig. 10C of Patel et al. discloses a method of modifying a set of available magnitudes (Col. 15 lines 50 – 55) of a bias voltage output signal [To Core] generated by a bias generator comprising (combination of [1050, 1055 and 1060-1064]): providing a metal-programmable transistor [1060, 1064] in the bias generator ([1060-1064] is in the combination of the bias generator [1050, 1055 and 1060-1064]); and metal programming (Fig. 10D, 10E) the metal-programmable transistor [1060, 1064] to connect the transistor to circuitry of the bias generator [1050, 1055 and 1060-1064], such that a corresponding ON state resistance of the metal-programmed transistor [1060, 1064] is combined with an effective ON state resistance of the circuitry (Fig. 10D, 10E) to modify the available magnitudes of the set (Col. 15 lines 50 – 55).

Regarding dependent claims 22 - 24, the claims incorporated substantial the same subject matter as of claims 3 and 4, and rejected along the same rationale.

Regarding dependent claim 25, Fig. 10C of Patel et al. discloses wherein providing a metal programmable transistors [1060, 1062] comprises providing either or both of a selection of metal-programmable pull-up transistors (Fig. 10D) and a selection of metal-programmable pull-down transistors (Fig. 10D) in the bias generator [1050, 1055 and 1060-1064], at least one of the metal-programmable transistors [1060] of each respective selection (Fig. 10D) being different from other metal-programmable transistors [1064] of the respective selections (Fig. 10E), and wherein metal programming the metal-programmable transistor (Fig. 10E, Fig. 10D) comprises selecting a respective metal-programmable transistor (Fig. 10E, 10D) from either or both the pull-up transistor selection and the pull-down transistor selection, and connecting the selected respective metal-programmable transistor (Fig. 10E, 10D) to the bias generator circuitry [1050, 1055 and 1060-1064].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable by Patel et al., U.S. patent No. 6,025,737 in further view of Ando U.S. Patent No. 6,560,142 – filed: Mar. 22, 2002.

Patel et al. as applied to claim 1 above, does not disclose the bias output signal (To Core) is biases a gate of a weak write pull-down transistor of a write driver in the memory (SRAM).

Fig. 1 of Ando discloses a bias signal (WW) is biasing a gate of a weak write pull down transistor (1) of a writer driver (WB) in the memory.

It is obvious to use the bias generator of Patel et al. in an environment where a driver of a memory is needed or a general combination of memory system elements to provide a particular end result. One a particular end result is known from the viewpoint of overall memory system, it would be obvious to use the particular circuit with specific components as discussed in Ando to meet refinement for that specific use. This refinement of known circuitry such as that taught in Ando is well known in the operating and use of memory circuitry in the production and manufacturing of a memory system and is considered to be routine part of the final stages prior to final preparation for sale and end use.

Allowable Subject Matter

4. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With regard to claims 9 and 10, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest “wherein the mode select input controls a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the bias generator output in the default mode”.

5. Claims 12 – 20 are allowed over prior art.

The following is a statement of reasons for the indication of allowable subject matter:

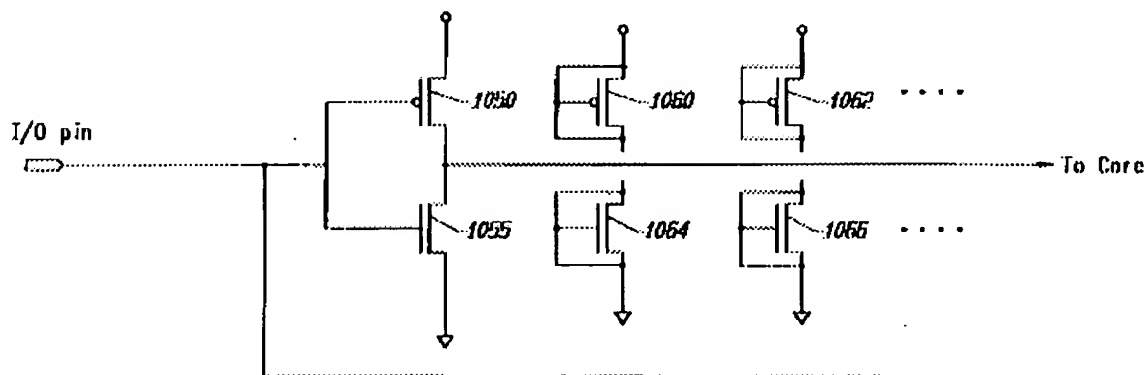
With regard to claims 12 and 17, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest “a bias generator having a first transistor having a source connected to drains of the pull-up transistor array, a drain connected to the bias generator output and a gate connected to an inverse mode select input; and a second transistor having a source connected to the second supply voltage, a drain connected to the bias generator output, and a gate connected to the inverse mode select input, wherein the mode select input and the inverse mode select input control a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the bias generator output in the default mode”.

Dependent claims 13 - 16 and 18 - 20 are allowed based on independent claims 12 and 17 above.

Response to Arguments

6. Applicant's arguments filed 12/21/05 have been fully considered but they are not persuasive.

7. Under remarks, with respect to claims 1, 6 and 21, applicant argued that Patel et al. does not disclose "a bias generator or an output thereof and means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal program". Examiner respectfully disagrees from the following: a bias signal is a signal uses to control or drive a circuit, and that well understood to one ordinary skill in the art.

***FIG. 10C***

Per explained above, Patel [1050 and 1055] clearly discloses a bias signal "To Core", because the signal "To Core" generating by 1050 and 1055 is using to drive and control the Core; thereby 1050/1055 is a generator.

Patel 's [1060, 1064] (Col. 15 lines 50-52 and 62-64) clearly disclose means (See Fig. 10D and 10E for disclosing adjusting the bias signal "To Core") for adjusting a set

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of available magnitudes (Fig. 10,D, 10E) at the output of a bias voltage output signal (To Core) at the output using metal programming (Col. 15 lines 48 - 53).

Fig. 10C of Patel clearly discloses a metal programmable transistor (1060, 1064, 1062, 1066) that adjusts a set of available magnitudes of a bias voltage output signal (To Core) at the bias generator (1050, 1055) when metal programmed (10E, 10D).

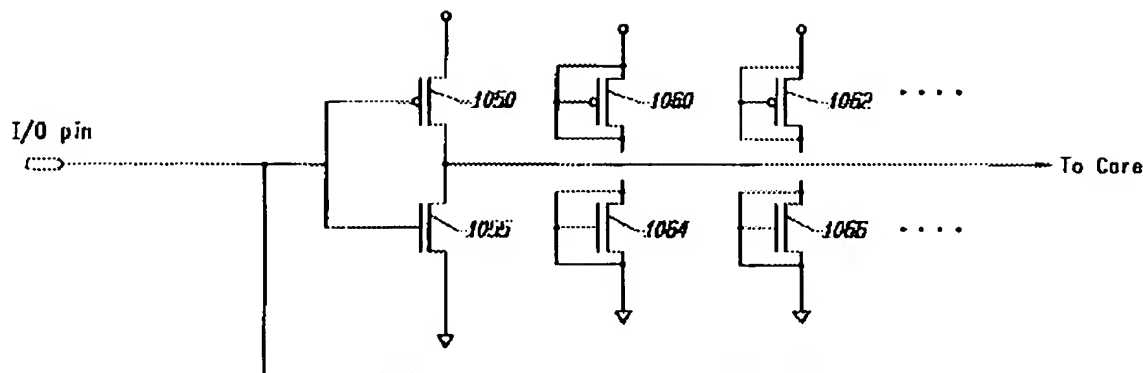
8. From previous office action, the word "test" is an intended of use because a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from prior art apparatus satisfying the claimed structural limitations.

9. Accordingly, the previous office action is applying to this office action.

Response to Arguments

10. Applicant's arguments filed 12/21/05 have been fully considered but they are not persuasive.

11. Under remarks, on page 13, with respect to claim 1, applicant argued that Patel et al. does not disclose a "bias generator" or an output thereof. Examiner respectful disagrees from the following:

*FIG. 10C*

Applicant's specification, Page 5, line 28 through page 6, line 9 teach bias generator produces as an output signal a bias voltage and the bias voltage has a magnitude that is selectable from among a set of available magnitude and magnitudes may be modified or adjusted using meta programming. Patel discloses inverting input buffer [1050 and 1055] has similar function as bias generator such as transistors [1050 and 1055] may be adjusted by programmable option and produces as an output signal to Core (see Fig. 10C above) and the bias voltage [voltage supplies and voltage levels] have a magnitude that is selectable from among a set of available magnitude and magnitudes may be modified or adjusted using meta programming (Patel, Col. 15 lines 33-46).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

14. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.


Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published

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applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.



Tuan T. Nguyen

Dang Nguyen 2/13/2006